

MC14514B, MC14515B

4-Bit Transparent Latch / 4-to-16 Line Decoder

The MC14514B and MC14515B are two output options of a 4 to 16 line decoder with latched inputs. The MC14514B (output active high option) presents a logical “1” at the selected output, whereas the MC14515B (output active low option) presents a logical “0” at the selected output. The latches are R–S type flip–flops which hold the last input data presented prior to the strobe transition from “1” to “0”. These high and low options of a 4–bit latch / 4 to 16 line decoder are constructed with N–channel and P–channel enhancement mode devices in a single monolithic structure. The latches are R–S type flip–flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load the Rated Temperature Range
- Pb–Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	–0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	–0.5 to V_{DD} +0.5	V
Input or Output Current (DC or Transient) per Pin	I_{in}, I_{out}	±10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	–55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Lead Temperature (8–Second Soldering)	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic “P and D/DW”
Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

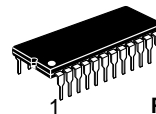
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



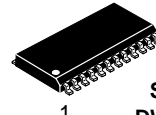
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MARKING DIAGRAMS



PDIP–24
P SUFFIX
CASE 709

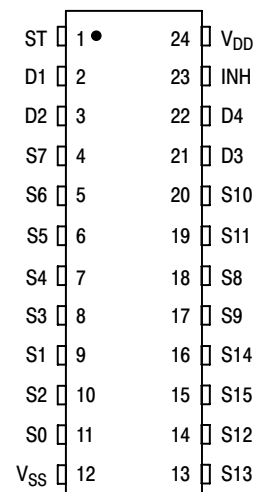


SOIC–24
DW SUFFIX
CASE 751E



xx = 14 or 15
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

PIN ASSIGNMENT



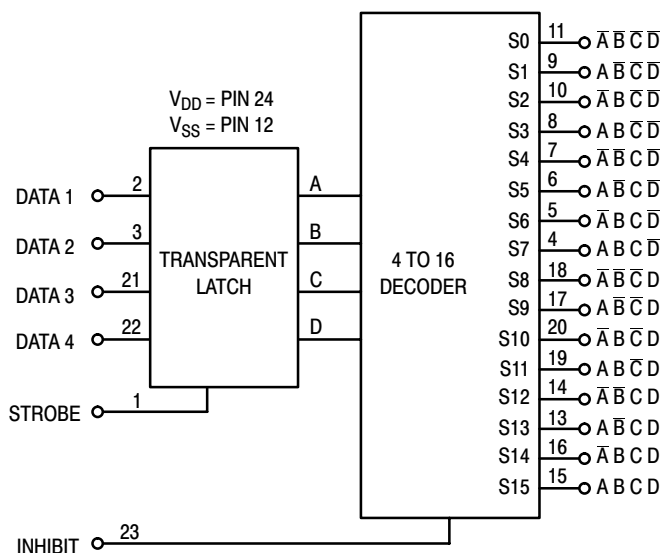
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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BLOCK DIAGRAM



DECODE TRUTH TABLE (Strobe = 1)*

Inhibit	Data Inputs				Selected Output MC14514 = Logic "1" MC14515 = Logic "0"
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care

*Strobe = 0, Data is latched

ORDERING INFORMATION

Device	Package	Shipping†
MC14514BCP	PDIP-24	15 Units / Rail
MC14514BCPG	PDIP-24 (Pb-Free)	
MC14514BDW	SOIC-24	30 Units / Rail
MC14514BDWR2	SOIC-24	1000 / Tape & Reel
MC14514BDWR2G	SOIC-24 (Pb-Free)	
MC14515BCP	PDIP-24	15 Units / Rail
MC14515BCPG	PDIP-24 (Pb-Free)	
MC14515BDW	SOIC-24	30 Units / Rail
MC14515BDWR2	SOIC-24	1000 / Tape & Reel
MC14515BDWR2G	SOIC-24 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0 $V_{in} = 0$ or V_{DD}	“0” Level V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
	“1” Level V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc) ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	“0” Level V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
	“1” Level V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc) ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	Source I_{OH}	5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	mAdc
		5.0	–0.25	–	–0.2	–0.36	–	–0.14	–	
		10	–0.62	–	–0.5	–0.9	–	–0.35	–	
		15	–1.8	–	–1.5	–3.5	–	–1.1	–	
	Sink I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
15		4.2	–	3.4	8.8	–	2.4	–		
Input Current	I_{in}	15	–	± 0.1	–	± 0.00001	± 0.1	–	± 1.0	μ Adc
Input Capacitance ($V_{in} = 0$)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μ Adc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_{TL}	5.0	$I_T = (1.35 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (2.70 \mu\text{A/kHz}) f + I_{DD}$ $I_T = (4.05 \mu\text{A/kHz}) f + I_{DD}$							μ Adc
		10								
		15								

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$ where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.002$.

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SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ (Note 6)	Max	
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	t_{TLH}	5.0 10 15	– – –	180 90 65	360 180 130	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time; Data, Strobe to S $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.86 \text{ ns/pF}) C_L + 192 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	– – –	550 225 150	1100 450 300	ns
Inhibit Propagation Delay Times $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	$t_{PLH},$ t_{PHL}	5.0 10 15	– – –	400 150 100	800 300 200	ns
Setup Time Data to Strobe	t_{su}	5.0 10 15	250 100 75	125 50 38	– – –	ns
Hold Time Strobe to Data	t_h	5.0 10 15	–20 0 10	–100 –40 –30	– – –	ns
Strobe Pulse Width	t_{WH}	5.0 10 15	350 100 75	175 50 38	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C .
 6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

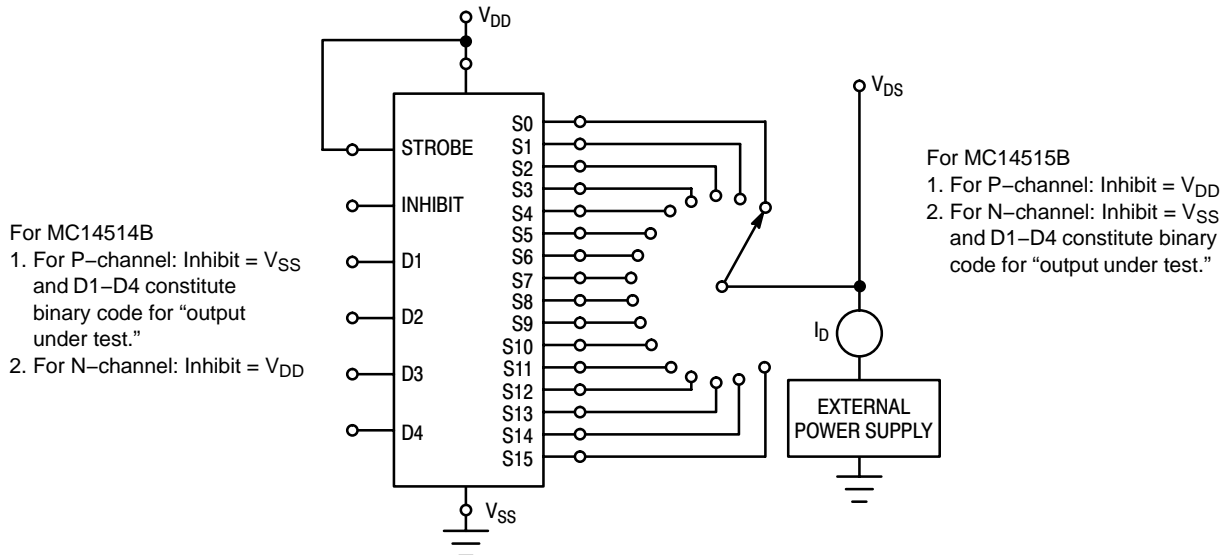


Figure 1. Drain Characteristics Test Circuit

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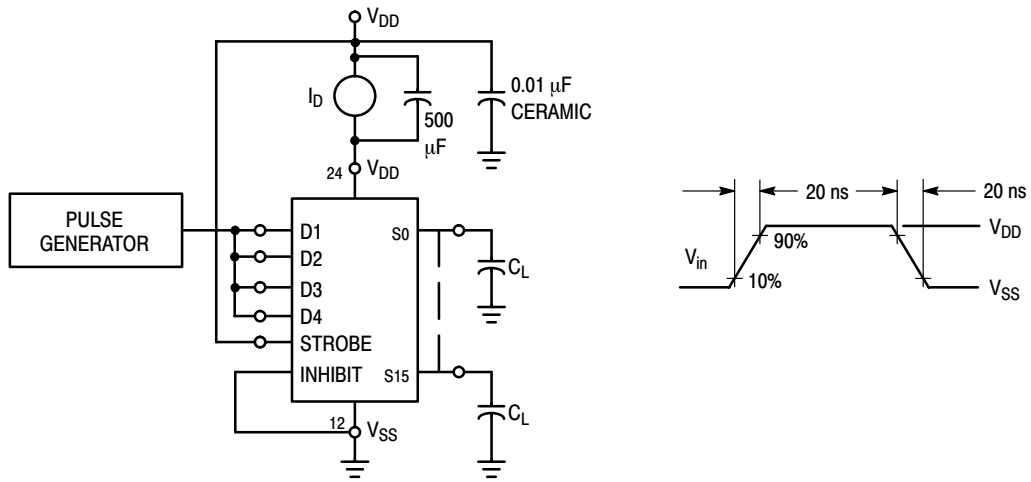


Figure 2. Dynamic Power Dissipation Test Circuit and Waveform

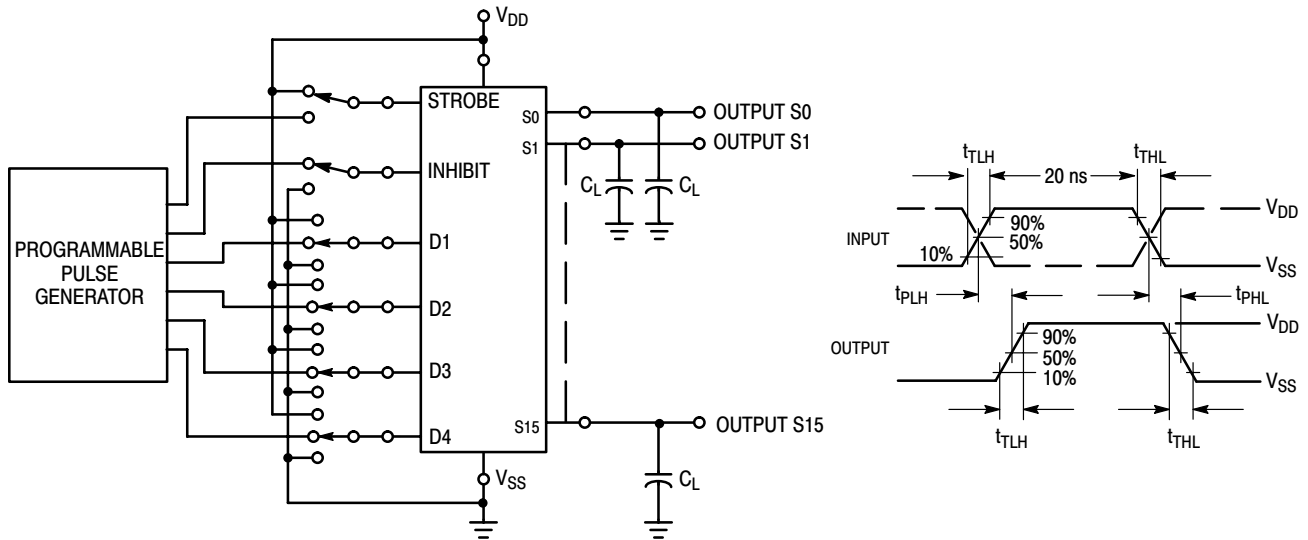
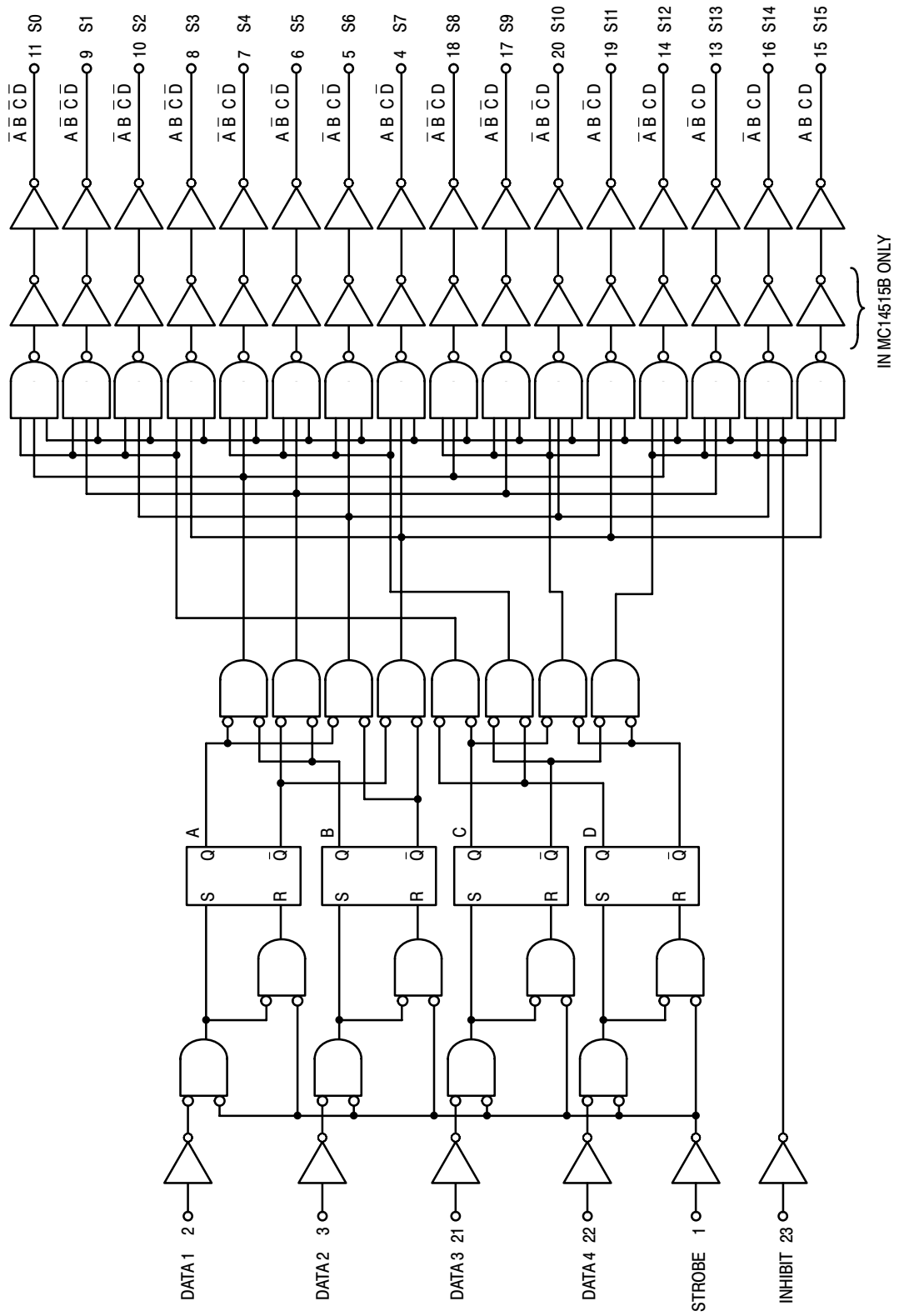


Figure 3. Switching Time Test Circuit and Waveforms

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LOGIC DIAGRAM



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COMPLEX DATA ROUTING

Two MC14512 eight-channel data selectors are used here with the MC14514B four-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

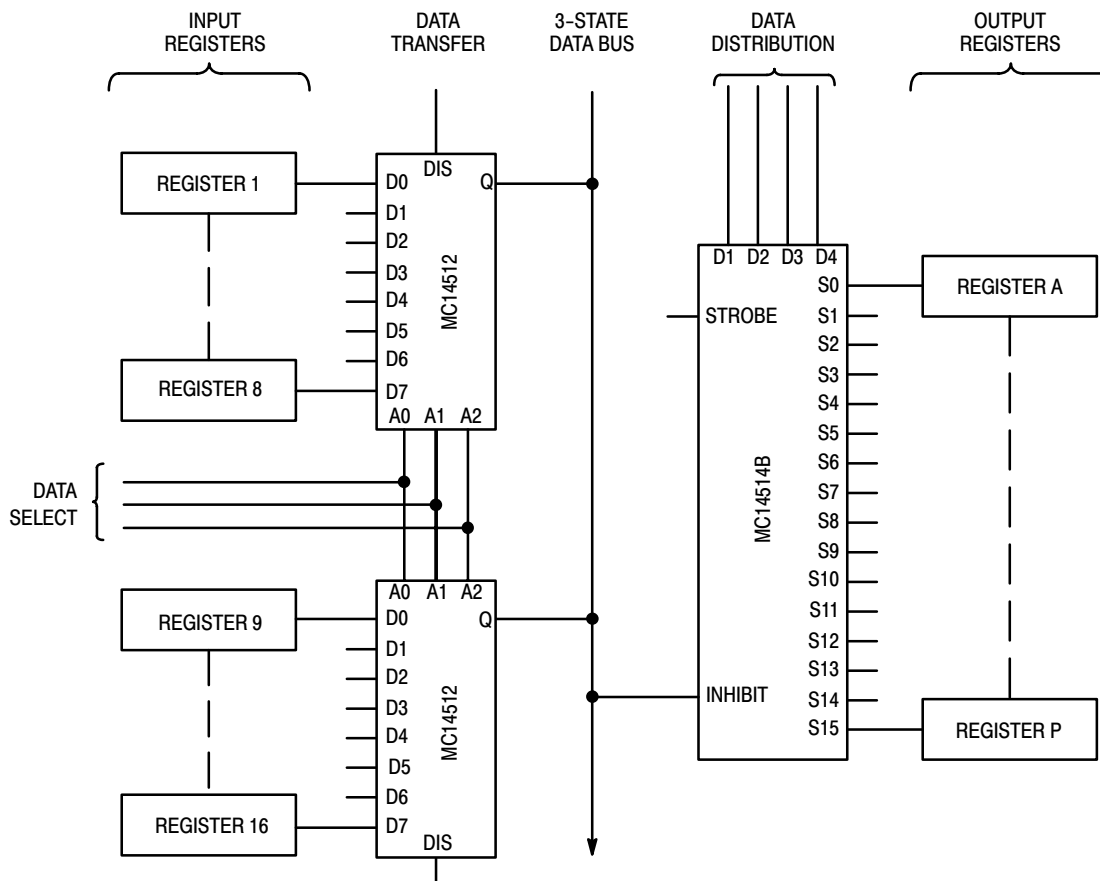
Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight

times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514B four-bit latch/decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

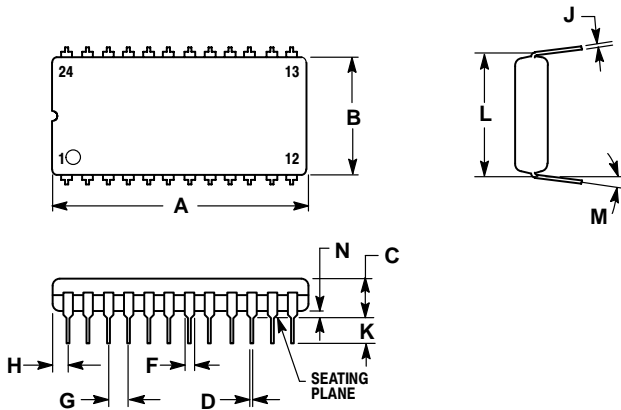
DATA ROUTING SYSTEM



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PACKAGE DIMENSIONS

PDIP-24 CASE 709-02 ISSUE D

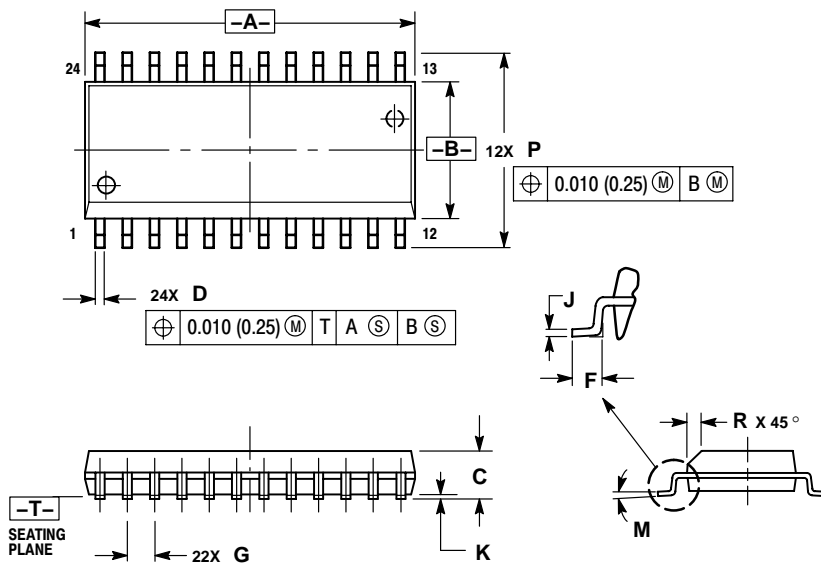


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.235	1.265	31.37	32.13
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.080	1.65	2.03
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

SOIC-24 CASE 751E-04 ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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